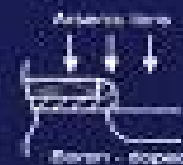
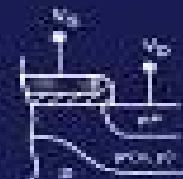
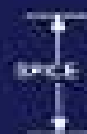


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COMPUTER SIMULATION OF IC PROCESSES AND DEVICES



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Zhiping Yu

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Emilie Sanchez



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digital MOS subcircuits which address a large number of shortcomings in existing digital MOS macromodels Specifically the
techniques address the device model detail transistor coupling capacitance effective channel length modulation series
transistor reduction effective transconductance input terminal dependence gate parasitic capacitance the body effect the
impact of parasitic RC interconnects and the effect of transmission gates The techniques address major sources of errors in
existing macromodeling techniques which must be addressed if macromodeling is to be accepted in commercial CAD tools by
chip designers The techniques presented in Chapters 4 6 can be implemented in other macromodels and are demonstrated
using the macromodel presented in Chapter 3 The new techniques are validated over an extremely wide range of operating
conditions much wider than has been presented for previous macromodels thus demonstrating the wide range of applicability
of these techniques **Electrical & Electronics Abstracts** ,1997 Predicasts F & S Index United States Predicasts,
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