

# **System Level Design Model with Reuse of System IP**

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# System Level Design Model With Reuse Of System Ip

**Y Pai**

A decorative graphic element consisting of a light blue horizontal bar with a rounded right end, and a red circular gradient shape partially visible behind it.

## **System Level Design Model With Reuse Of System Ip:**

**System Level Design Model with Reuse of System IP** Patrizia Cavalloro, Christophe Gendarme, Klaus Kronlöf, Jean Mermet, J. van Sas, Kari Tiensyrjä, Nikolaos Voros, 2003-09-30 This book addresses system design providing a framework for assessing and developing system design practices that observe and utilise reuse of system design know how The know how accumulated in the companies represents an intellectual asset or property IP *Proceedings of ASP-DAC/VLSI Design 2002*, 2002 Papers from a January 2002 conference are organized into four sessions each on low power design synthesis testing layout and interconnects and technology as well as two sessions each on embedded systems verification and VLSI architecture one session on analog design and one session on hot c *Proceedings of the ASP-DAC ... Asia and South Pacific Design Automation Conference*, 2002 **Optimizing Mapping in System Level Design** Qi Zhu, 2008 IEEE International High-Level Design Validation and Test Workshop, 2003 **International Symposium on System Synthesis**, 2002 **Information Society Technologies**, 2000 *Business Periodicals Index*, 2000 System-on-a-chip Rochit Rajsuman, 2000 Starting with a basic overview of system on a chip SoC including definitions of related terms this new book helps you understand SoC design challenges and the latest design and test methodologies You see how ASIC technology evolved to an embedded cores based concept that includes pre designed reusable Intellectual Property IP cores that act as microprocessors data storage devices DSP bus control and interfaces all stitched together by a User s Defined Logic UDL

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