

System Synthesis with VHDL

Petru Eles, Krzysztof Kuchcinski and Zebo Peng

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System Synthesis With Vhdl A Transformational Approach

Michael Rajnik



System Synthesis With Vhdl A Transformational Approach:

System Synthesis with VHDL Petru Eles, Krzysztof Kuchcinski, Zebo Peng, 2013-03-14 Embedded systems are usually composed of several interacting components such as custom or application specific processors ASICs memory blocks and the associated communication infrastructure The development of tools to support the design of such systems requires a further step from high level synthesis towards a higher abstraction level The lack of design tools accepting a system level specification of a complete system which may include both hardware and software components is one of the major bottlenecks in the design of embedded systems Thus more and more research efforts have been spent on issues related to system level synthesis This book addresses the two most active research areas of design automation today high level synthesis and system level synthesis In particular a transformational approach to synthesis from VHDL specifications is described System Synthesis with VHDL provides a coherent view of system synthesis which includes the high level and the system level synthesis tasks VHDL is used as a specification language and several issues concerning the use of VHDL for high level and system level synthesis are discussed These include aspects from the compilation of VHDL into an internal design representation to the synthesis of systems specified as interacting VHDL processes The book emphasizes the use of a transformational approach to system synthesis A Petri net based design representation is rigorously defined and used throughout the book as a basic vehicle for illustration of transformations and other design concepts Iterative improvement heuristics such as tabu search simulated annealing and genetic algorithms are discussed and illustrated as strategies which are used to guide the optimization process in a transformation based design environment Advanced topics including hardware software partitioning test synthesis and low power synthesis are discussed from the perspective of a transformational approach to system synthesis System Synthesis with VHDL can be used for advanced undergraduate or graduate courses in the area of design automation and more specifically of high level and system level synthesis At the same time the book is intended for CAD developers and researchers as well as industrial designers of digital systems who are interested in new algorithms and techniques supporting modern design tools and methodologies **System Synthesis with**

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Prototyping Rudy Lauwereins, 1995 To help designers and developers of hardware software systems knock together a working model more quickly the 33 papers discuss models for system simulation and emulation in a hierarchical sense software to hardware mapping software prototyping and validation prototyping environments of hardware Practical Formal Methods for Hardware Design Carlos Delgado Kloos, Werner Damm, 2012-12-06 Formal methods for hardware design still find limited use in industry Yet current practice has to change to cope with decreasing design times and increasing quality requirements This research report presents results from the Esprit project FORMAT formal methods in hardware verification which involved the collaboration of the enterprises Siemens Italtel Telefonica I D TGI and AHL the research

institute OFFIS and the universities of Madrid and Passau The work presented involves advanced specification languages for hardware design that are intuitive to the designer like timing diagrams and state based languages as well as their relation to VHDL and formal languages like temporal logic and a process algebraic calculus The results of experimental tests of the tools are also presented *Proceedings of the Third International Workshop on Hardware/Software Codesign*, 1994 The proceedings of the September 1994 workshop comprise 28 technical papers that represent several important trends in co design research use of design case studies to drive research algorithms for hardware software partitioning algorithms for system verification and validation and a continuing interest in design representations No index Annotation copyright by Book News Inc Portland OR *EDA for IC System Design, Verification, and Testing* Louis Scheffer, Luciano Lavagno, Grant Martin, 2018-10-03 Presenting a comprehensive overview of the design automation algorithms tools and methodologies used to design integrated circuits the Electronic Design Automation for Integrated Circuits Handbook is available in two volumes The first volume EDA for IC System Design Verification and Testing thoroughly examines system level design microarchitectural design logical verification and testing Chapters contributed by leading experts authoritatively discuss processor modeling and design tools using performance metrics to select microprocessor cores for IC designs design and verification languages digital simulation hardware acceleration and emulation and much more Save on the complete set

High-Level Verification Sudipta Kundu, Sorin Lerner, Rajesh K. Gupta, 2011-05-18 Given the growing size and heterogeneity of Systems on Chip SOC the design process from initial specification to chip fabrication has become increasingly complex This growing complexity provides incentive for designers to use high level languages such as C SystemC and SystemVerilog for system level design While a major goal of these high level languages is to enable verification at a higher level of abstraction allowing early exploration of system level designs the focus so far for validation purposes has been on traditional testing techniques such as random testing and scenario based testing This book focuses on high level verification presenting a design methodology that relies upon advances in synthesis techniques as well as on incremental refinement of the design process These refinements can be done manually or through elaboration tools This book discusses verification of specific properties in designs written using high level languages as well as checking that the refined implementations are equivalent to their high level specifications The novelty of each of these techniques is that they use a combination of formal techniques to do scalable verification of system designs completely automatically The verification techniques presented in this book include methods for verifying properties of high level designs and methods for verifying that the translation from high level design to a low level Register Transfer Language RTL design preserves semantics Used together these techniques guarantee that properties verified in the high level design are preserved through the translation to low level RTL **EUROMICRO 96** Peter Milligan, Krzysztof Kuchcinski, 1996 *Proceedings Euromicro. Conference*, 1998

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Makuhari Messe, Nippon Convention Center, Chiba, Japan IEEE Circuits and Systems Society, 1996 The Asia and South Pacific conference on design automation is the second in a series of biennial international conferences It aims to provide the CAD DA community with the opportunity to present ideas and concepts on upstream design as well as methodologies of downstream design

Computing in Research and Development in Africa Abdoulaye Gamatié, 2014-10-11 This book describes the trends challenges and solutions in computing use for scientific research and development within different domains in Africa such as health agriculture environment economy energy education and engineering The benefits expected are discussed by a number of recognized domain specific experts with a common theme being computing as solution enabler This book is the first document providing such a representative up to date view on this topic at the continent level

Readings in Hardware/Software Co-Design Giovanni De Micheli, Rolf Ernst, Wayne Wolf, 2002 This title serves as an introduction and reference for the field with the papers that have shaped the hardware software co design since its inception in the early 90s

Languages for System Specification Christoph Grimm, 2007-05-08 Contributions on UML address the application of UML in the specification of embedded HW SW systems C Based System Design embraces the modeling of operating systems modeling with different models of computation generation of test patterns and experiences from case studies with SystemC Analog and Mixed Signal Systems covers rules for solving general modeling problems in VHDL AMS modeling of multi nature systems synthesis and modeling of Mixed Signal Systems with SystemC Languages for formal methods are addressed by contributions on formal specification and refinement of hybrid embedded and real time stems Together with articles on new languages such as SystemVerilog and Software Engineering in Automotive Systems the contributions selected for this book embrace all aspects of languages and models for specification design modeling and verification of systems Therefore the book gives an excellent overview of the actual state of the art and the latest research results

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Journal of VLSI Signal Processing Systems for Signal, Image, and Video Technology, 2007

Software Systems in Engineering, 1995 Daniel Cooke, 1995

Proceedings, 1995

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web for flanges with 12 or more bolts 1 st round 20 percent of final torque 2 nd round 40 percent of final torque 3 rd round 80 percent of final torque 4 th round 100 percent of final torque final round clockwise or counter clockwise around the flange please take note the above bolt tightening sequences are the most

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