



# System Level Design Of Reconfigurable Systems On Chips

**Nikolaos Voros, Alberto Rosti, Michael  
Hübner**



## **System Level Design Of Reconfigurable Systems On Chips:**

**System Level Design of Reconfigurable Systems-on-Chip** Nikolaos Voros, Konstantinos Masselos, 2006-02-23 System Level Design of Reconfigurable Systems on Chip provides insight in the challenges and difficulties encountered during the design of reconfigurable Systems on Chip SoCs Reconfiguration is becoming an important part of System on Chip design to cope with the increasing demands for simultaneous flexibility and computational power The book focuses on system level design issues for reconfigurable SoCs and provides information on reconfiguration aspects of complex SoCs and how they can be implemented in practice It is divided in three parts The first part provides background information and requirements on reconfigurable technologies and systems The second one identifies existing methodological gaps and introduces a design flow for developing reconfigurable Systems on Chip The high level part of the design flow can be covered by two C based methodologies one based on SystemC and one based on OCAPI XL both including appropriate extensions to handle reconfiguration issues Finally the third part of the book presents reconfigurable SoCs from the perspective of the designer through three indicative case studies from the wireless and multimedia communication domain *Dynamic System*

*Reconfiguration in Heterogeneous Platforms* Nikolaos Voros, Alberto Rosti, Michael Hübner, 2009-05-28 Dynamic System Reconfiguration in Heterogeneous Platforms defines the MORPHEUS platform that can join the performance density advantage of reconfigurable technologies and the easy control capabilities of general purpose processors It consists of a System on Chip made of a scalable system infrastructure hosting heterogeneous reconfigurable accelerators providing dynamic reconfiguration capabilities and data stream management capabilities Dynamic Reconfigurable Network-on-Chip

Design: Innovations for Computational Processing and Communication Shen, Jih-Sheng, Hsiung, Pao-Ann, 2010-06-30 Reconfigurable computing brings immense flexibility to on chip processing while network on chip has improved flexibility in on chip communication Integrating these two areas of research reaps the benefits of both and represents the promising future of multiprocessor systems on chip This book is the one of the first compilations written to demonstrate this future for network on chip design Through dynamic and creative research into questions ranging from integrating reconfigurable computing techniques to task assigning scheduling and arrival to designing an operating system to take advantage of the computing and communication flexibilities brought about by run time reconfiguration and network on chip it represents a complete source of the techniques and applications for reconfigurable network on chip necessary for understanding of future of this field **The Design and Implementation of a 200k-gate Reconfigurable Computing System** Feng Yun, 1997

**Introduction to Reconfigurable Computing** Christophe Bobda, 2007-09-30 Introduction in Reconfigurable Computing provides a comprehensive study of the field Reconfigurable Computing It provides an entry point to the novice willing to move in the research field reconfigurable computing FPGA and system on programmable chip design The book can also be used as teaching reference for a graduate course in computer engineering or as reference to advance electrical and

computer engineers It provides a very strong theoretical and practical background to the field of reconfigurable computing from the early Estrin's machine to the very modern architecture like coarse grained reconfigurable device and the embedded logic devices Apart from the introduction and the conclusion the main chapter of the book are the following Architecture of reconfigurable systems which presents the technology and the architecture used in fine grained and those used in coarse grained reconfigurable devices Design and implementation This section deals with the implementation on reconfigurable system It briefly covers the steps needed to implement application on today's FPGAs And focus on the logic synthesis for FPGA in particular LUT technology mapping High Level Synthesis for Reconfigurable Devices The high level synthesis for reconfigurable systems also known as temporal partitioning is presented here Several temporal partitioning techniques are presented and explained Temporal placement This section considers stand alone reconfigurable systems Its assume that a kind of operating systems for reconfigurable systems is in charge of managing the resources of a given system and allocate space on a device for the computation of incoming tasks and therefore presents several temporal placement approaches for off line as well as on line placement On line and Dynamic Interconnection This chapter reviews and explains the different approaches for allowing communication between modules dynamically placed at run time on a given device Designing a reconfigurable application on Xilinx Virtex FPGA In this section the different design approaches of partial reconfigurable systems on the Xilinx FPGAs that are one of the few one on the market with this feature is explained System on programmable chip System on programmable chip is a hot topic in reconfigurable computing This is mainly the integration of a system made upon some peripheral UART Ethernet VGA etc but also computational Coding filter etc hardware modules on one programmable chip The current usable solutions are presented The book furthermore focusses on the development of adaptive multiprocessors on chip i.e systems consisting of a set of Processors and exchangeable hardware accelerators Applications This part covers the use of reconfigurable system in computer architecture rapid prototyping reconfigurable supercomputer reconfigurable massively parallel computers and algorithm better adapted for reconfigurable systems distributed arithmetic network packet processing etc *Proceedings of ASP-DAC/VLSI Design 2002*, 2002 Papers from a January 2002 conference are organized into four sessions each on low power design synthesis testing layout and interconnects and technology as well as two sessions each on embedded systems verification and VLSI architecture one session on analog design and one session on hot c *Proceedings of the 2002 International Workshop on System-level Interconnect Prediction*, 2002 **Proceedings of the ASP-DAC ... Asia and South Pacific Design Automation Conference**, 2002 **Parallel and Distributed Processing**, 1998 **System-level Exploration for Pareto-optimal Configurations in Parameterized System-on-a-chip Architectures** Tony Digaleh Givargis, 2001 First IEEE/ACM/IFIP International Conference on Hardware/Software Codesign & System Synthesis, 2003 *Embedded Systems Programming*, 1998-07 **IEEE Circuits & Devices**, 2006 **Proceedings**, 1983 **IEEE Computer Society Workshop on VLSI**

**2000** Asim Smailagic, Robert W. Brodersen, H. De Man, 2000 Contains 23 papers from the April 2000 workshop which identified system level design as a dominant VLSI research theme for the next decade System design is converging on a model which combines general purpose commodity chips and full custom mixed analogy with digital application specific integrated circuits integrated via programmable gate arrays on custom printed circuit boards or complete silicon boards creating a system on a chip Some of the papers discuss the constraints of complexity power consumption heat dissipation mechanical packaging ergonomics and design effort Other major topics are timing issues analysis and synthesis of asynchronous circuits and advances in multiplier design No subject index Annotation copyrighted by Book News Inc Portland OR

**VLSI: Systems on a Chip** Luis Miguel Silveira, Srinivas Devadas, Ricardo A. Reis, 1999-12-31 The current trend towards the realization of complex and versatile Systems on a Chip requires the combined efforts and attention of experts in a wide range of areas including microsystems embedded hardware software systems dedicated ASIC and programmable logic hardware reconfigurable computing wireless communications and RF issues video and image processing memory systems low power design techniques design test and verification algorithms modeling and simulation logic synthesis and interconnect analysis Thus the contributions presented herein address a wide range of Systems on a Chip problems VLSI Systems on a Chip comprises the selected proceedings of the Tenth International Conference on Very Large Scale Integration VLSI 99 which was sponsored by the International Federation for Information Processing IFIP and was held in Lisbon Portugal in December 1999 The volume is organized around two themes in which the following topics are addressed VLSI Systems Design and Applications Analog Systems Design Analog Modeling and Design Image Processing Reconfigurable Computing Memory and System Design Low Power Design VLSI Design Methods and CAD Test and Verification Analog CAD and Interconnect Fundamental CAD Algorithms Verification and Simulation CAD for Physical Design High Level Synthesis and Verification of Embedded Systems VLSI Systems on a Chip is essential reading for researchers working on system integration design and CAD

**Journal of VLSI Signal Processing Systems for Signal, Image, and Video Technology**, 1999

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*2001 International Conference on Modeling and Simulation of Microsystems* Matthew Laudon, Bartlomiej F. Romanowicz, 2001 The worlds most comprehensive and up to date collection of Multidisciplinary Micro and Nano technical papers Technical Proceedings of the 2001 International Conference on Modeling and Simulation of Microsystems Micro and Nano Fluidic Systems MEMS System Optimization MEMS Applications and Characterization Advanced Numerics Process Modeling Quantum Effects Quantum Devices Spintronics Atomistic of Silicon Processing Advanced Semiconductors Circuit Modeling Compact Modeling Papers taken from the 2001 MSM Hilton Head Island USA March 2001

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