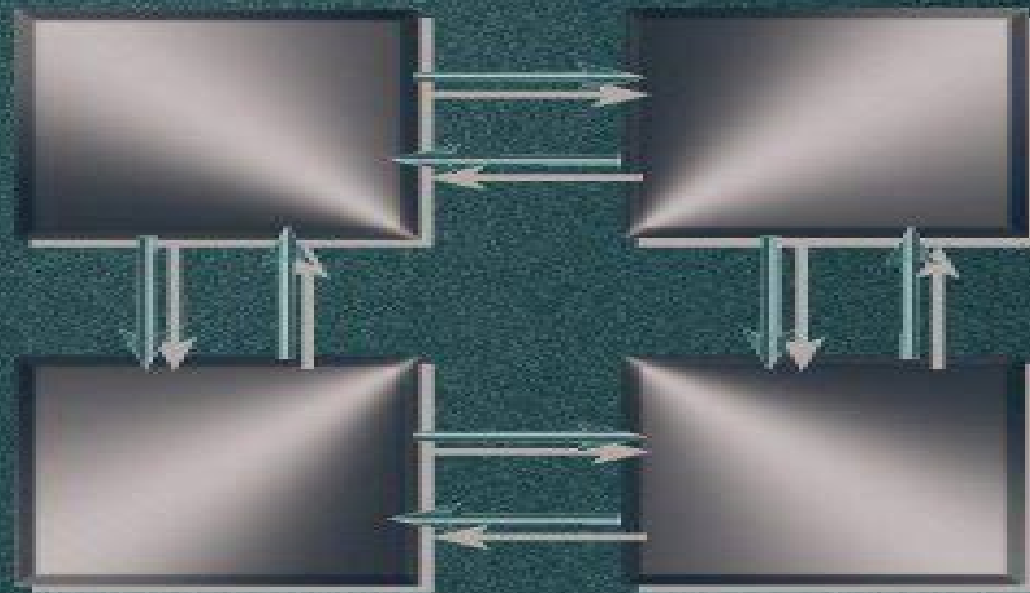


# Specification and Verification of Systolic Arrays



**Nam Ling & Magdy A Bayoumi**

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# Specification And Verification Of Systolic Arrays

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## **Specification And Verification Of Systolic Arrays:**

**Specification And Verification Of Systolic Arrays** Magdy A Bayoumi, Nam Ling, 1999-08-05 Circuits and architectures have become more complex in terms of structure interconnection topology and data flow Design correctness has become increasingly significant as errors in design may result in strenuous debugging or even in the repetition of a costly manufacturing process Although circuit simulation has been used traditionally and widely as the technique for checking hardware and architectural designs it does not guarantee the conformity of designs to specifications Formal methods therefore become vital in guaranteeing the correctness of designs and have thus received a significant amount of attention in the CAD industry today This book presents a formal method for specifying and verifying the correctness of systolic array designs Such architectures are commonly found in the form of accelerators for digital signal image and video processing These arrays can be quite complicated in topology and data flow In the book a formalism called STA is defined for these kinds of dynamic environments with a survey of related techniques A framework for specification and verification is established Formal verification techniques to check the correctness of the systolic networks with respect to the algorithmic level specifications are explained The book also presents a Prolog based formal design verifier named VSTA developed to automate the verification process as using a general purpose theorem prover is usually extremely time consuming Several application examples are included in the book to illustrate how formal techniques and the verifier can be used to automate proofs

Proceedings of the 1993 International Conference on Parallel Processing Alok N. Choudhary, P. Bruce Berra, 1993-08-16 This three volume work presents a compendium of current and seminal papers on parallel distributed processing offered at the 22nd International Conference on Parallel Processing held August 16 20 1993 in Chicago Illinois Topics include processor architectures mapping algorithms to parallel systems performance evaluations fault diagnosis recovery and tolerance cube networks portable software synchronization compilers hypercube computing and image processing and graphics Computer professionals in parallel processing distributed systems and software engineering will find this book essential to their complete computer reference library **Transformational Approaches to Systolic Design** G. M. Megson, 1994 Computer Systems Organization Processor Architectures *Proceedings of the International Conference on Application Specific Array Processors, September 2-4, 1991, Barcelona, Spain* Mateo Valero, 1991 The International Conference on Application Specific Array Processors ASAP 91 was held September 1991 in Barcelona Spain Application specific computing may be the solution to many computationally intensive problems Coverage here includes design mapping techniques synthesis and verification and systolic array designs and design methodologies No index Annotation copyrighted by Book News Inc Portland OR

*Computer Hardware Description Languages and their Applications* D. Agnew, L. Claesen, R. Camposano, 2014-05-21 Hardware description languages HDLs have established themselves as one of the principal means of designing electronic systems The interest in and usage of HDLs continues to spread rapidly driven by the increasing complexity of systems the

growth of HDL driven synthesis the research on formal design methods and many other related advances This research oriented publication aims to make a strong contribution to further developments in the field The following topics are explored in depth BDD based system design and analysis system level formal verification formal reasoning on hardware languages for protocol specification VHDL HDL based design methods high level synthesis and text graphical HDLs There are short papers covering advanced design capture and recent work in high level synthesis and formal verification In addition several invited presentations on key issues discuss and summarize recent advances in real time system design automatic verification of sequential circuits and languages for protocol specification

Proceedings of the ISMM International Conference: Parallel and Distributed Computing, and Systems R. Melhem,1992 *PARLE '92, Parallel Architectures and Languages Europe*

Daniel Etiemble,1992 The 1992 Parallel Architectures and Languages Europe conference continues the tradition of a wide and representative international meeting of specialists from academia and industry in theory design and application of parallel computer systems set by the previous PARLE conferences held in Eindhoven in 1987 1989 and 1991 This volume contains the 52 regular and 25 poster papers that were selected from 187 submitted papers for presentation and publication In addition five invited lectures are included The regular papers are organized into sections on implementation of parallel programs graph theory architecture optimal algorithms graph theory and performance parallel software components data base optimization and modeling data parallelism formal methods systolic approach functional programming fine grain parallelism Prolog data flow systems network efficiency parallel algorithms cache systems implementation of parallel languages parallel scheduling in data base systems semantic models parallel data base machines and language semantics PUBLISHER S WEBSITE Proceedings of the ... International IEEE Conference on Tools for Artificial Intelligence ,1991

**Protocol Specification, Testing and Verification, X** Luigi Logrippo,Robert L. Probert,Hasan Ural,1990 The contributions to this book are from researchers and practitioners concerned with the theory and application of formal methods to the specification testing and verification of protocols for open systems Being the tenth in a successful series of symposia a special feature of the book is a number of invited papers on the same theme The First Ten Years The Next Ten Years International Aerospace Abstracts ,1996 **Electrical & Electronics Abstracts** ,1997 *Proceedings of the ... Midwest Symposium on Circuits and Systems* ,1993 *Dissertation Abstracts International* ,1993 *VLSI Signal Processing* Peter R. Cappello,1984 Proceedings of the 31st Midwest Symposium on Circuits and Systems, August 9-12, 1988, Marriott's Pavilion Hotel, St. Louis, Missouri Linda R. Laub,R. Eugene Stuffle,University of Missouri--Rolla.

Engineering Continuing Education,University of Missouri--Rolla. Dept. of Electrical Engineering,1988 *Science Abstracts* ,1995 Вычислительные Машины И Искусственный Интеллект ,1993 **Proceedings of the ... International**

**Conference on Parallel and Distributed Information Systems** ,1992 **VLSI Signal Processing, II** Sun Yuan

Kung,Robert E. Owen,J. Greg Nash,1986 Formal VLSI Specification and Synthesis Luc J. M. Claesen,1990 Functional and

behavioral verification of correctness forms the bottleneck in current VLSI design systems For economical reasons design of VLSI circuits must be completely validated before manufacturing Current VLSI validation is mainly done through extensive simulation The emerging alternative is based on formal design and verification methods that guarantee correctness This book describes original work in all aspects of formal hardware design methods Topics covered include high level specification hardware description languages formal hardware verification methods guided synthesis methods correctness preserving transformations use of theorem provers for verification formal proof of correctness MOS timing verification methods design for verifiability and practical experiences

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