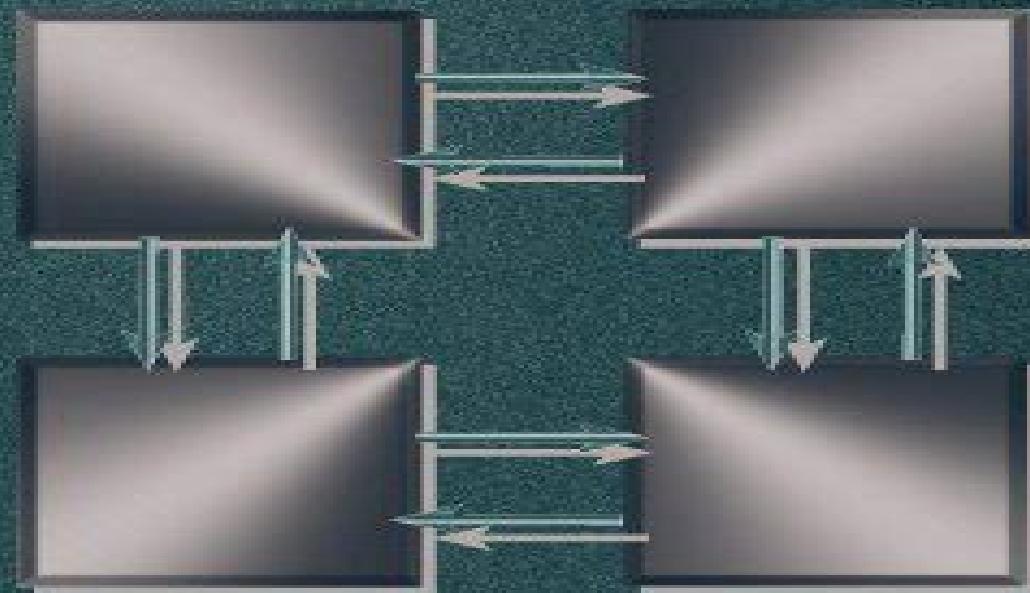


Specification and Verification of Systolic Arrays



Nam Ling & Magdy A Bayoumi

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Specification And Verification Of Systolic Arrays Magdy A Bayoumi,Nam Ling,1999-08-05 Circuits and architectures have become more complex in terms of structure interconnection topology and data flow Design correctness has become increasingly significant as errors in design may result in strenuous debugging or even in the repetition of a costly manufacturing process Although circuit simulation has been used traditionally and widely as the technique for checking hardware and architectural designs it does not guarantee the conformity of designs to specifications Formal methods therefore become vital in guaranteeing the correctness of designs and have thus received a significant amount of attention in the CAD industry today This book presents a formal method for specifying and verifying the correctness of systolic array designs Such architectures are commonly found in the form of accelerators for digital signal image and video processing These arrays can be quite complicated in topology and data flow In the book a formalism called STA is defined for these kinds of dynamic environments with a survey of related techniques A framework for specification and verification is established Formal verification techniques to check the correctness of the systolic networks with respect to the algorithmic level specifications are explained The book also presents a Prolog based formal design verifier named VSTA developed to automate the verification process as using a general purpose theorem prover is usually extremely time consuming Several application examples are included in the book to illustrate how formal techniques and the verifier can be used to automate proofs

Proceedings of the 1993 International Conference on Parallel Processing Alok N. Choudhary,P. Bruce Berra,1993-08-16 This three volume work presents a compendium of current and seminal papers on parallel distributed processing offered at the 22nd International Conference on Parallel Processing held August 16 20 1993 in Chicago Illinois Topics include processor architectures mapping algorithms to parallel systems performance evaluations fault diagnosis recovery and tolerance cube networks portable software synchronization compilers hypercube computing and image processing and graphics Computer professionals in parallel processing distributed systems and software engineering will find this book essential to their complete computer reference library

Transformational Approaches to Systolic Design G. M. Megson,1994 Computer Systems Organization Processor Architectures *Proceedings of the International Conference on Application Specific Array Processors, September 2-4, 1991, Barcelona, Spain* Mateo Valero,1991 The International Conference on Application Specific Array Processors ASAP 91 was held September 1991 in Barcelona Spain Application specific computing may be the solution to many computationally intensive problems Coverage here includes design mapping techniques synthesis and verification and systolic array designs and design methodologies No index Annotation copyrighted by Book News Inc Portland OR

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behavioral verification of correctness forms the bottleneck in current VLSI design systems. For economical reasons design of VLSI circuits must be completely validated before manufacturing. Current VLSI validation is mainly done through extensive simulation. The emerging alternative is based on formal design and verification methods that guarantee correctness. This book describes original work in all aspects of formal hardware design methods. Topics covered include high level specification, hardware description languages, formal hardware verification methods, guided synthesis methods, correctness preserving transformations, use of theorem provers for verification, formal proof of correctness, MOS timing verification methods, design for verifiability and practical experiences.

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