**NOTE:**
- If a candidate answers a question/vraag TWICE, only mark the FIRST attempt.
- Consistent accuracy applies in all aspects of the marking memorandum.

**LET WEL:**
- Indien 'n kandidaat 'n vraag TWEE keer beantwoord, merk slegs die EERSTE poging.
- Volgehoue akkuraatheid is DEURGAANS in ALLE aspekte van die memorandum van toepassing.

## QUESTION/VRAAG 1

| 1.1.1 | $3x^2 - 4x = 0$ <br><br> $x(3x - 4) = 0$ <br><br> $x = \dfrac{4}{3}$ or $x = 0$ | ✓ factors <br> ✓ both answers <br><br> (2) |
|---|---|---|
| 1.1.2 | $x - 6 + \dfrac{2}{x} = 0$ <br><br> $x^2 - 6x + 2 = 0$ <br><br> $x = \dfrac{-(-6) \pm \sqrt{(-6)^2 - 4(1)(2)}}{2(1)}$ <br><br> $= \dfrac{6 \pm \sqrt{28}}{2}$ <br><br> $x = 0{,}35$ or $x = 5{,}65$ <br><br> **OR** <br><br> $x - 6 + \dfrac{2}{x} = 0$ <br><br> $x^2 - 6x + 2 = 0$ <br><br> $(x - 3)^2 = -2 + 9$ <br><br> $(x - 3) = \pm\sqrt{7}$ <br><br> $x = 3 \pm \sqrt{7}$ <br><br> $x = 0{,}35$ or $x = 5{,}65$ | ✓ $x^2 - 6x + 2 = 0$ <br><br> ✓ subs into <br> correct formula <br> ✓ $x = 0{,}35$ <br> ✓ $x = 5{,}65$ <br><br> (4) <br><br><br><br> ✓ $x^2 - 6x + 2 = 0$ <br> ✓ $(x - 3)^2 = -2 + 9$ <br><br> ✓ $x = 0{,}35$ <br> ✓ $x = 5{,}65$ <br><br> (4) |
| 1.1.3 | $x^{\frac{2}{3}} = 4; \quad x > 0$ <br><br> $x = \left(2^2\right)^{\frac{3}{2}}$ <br><br> $x = 8$ <br><br> **OR** | ✓ $x = \left(2^2\right)^{\frac{3}{2}}$ <br><br><br> ✓ $x = 8$ <br><br> (2) |

# 2014 Exemplar Grade 12

**Lingsheng Yao**

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web as an alternative you can also write your simulation stimulus using generic vhdl code called a testbench the testbench codes gets compiled along with the design so that the stimulus is also in the compiled simulation model ieee came along and created additional libaries that are supported by almost all vhdl compilers specific silicon

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web for sample syntax and a list of vhdl statements supported by the vhdl synthesizer see appendix a quick reference for a list of exceptions and constraints on the vhdl synthesizer s support of vhdl see appendix b limitations this chapter shows you the structure of a vhdl design and then

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complex programmable logic device cpld development board

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to describe the input and output ports of this circuit 1 entity circuit 1 is 2 port a in std logic 3 b in std logic 4 out1 out std logic 5 end circuit 1

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web basic logic gates esd chapter 2 figure 2 3 every vhdl design description consists of at least one entity architecture pair or one entity with multiple architectures the entity section of the hdl design is used to declare the i o ports of the circuit while the description code resides within architecture portion

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web quartus and vhdl code in this section you should learn how to implement a vhdl code for single cycle data path before we go any further let s define some of the terms that we use throughout the book entity all designs are expressed in terms of entities an entity is the most basic building block in a design

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