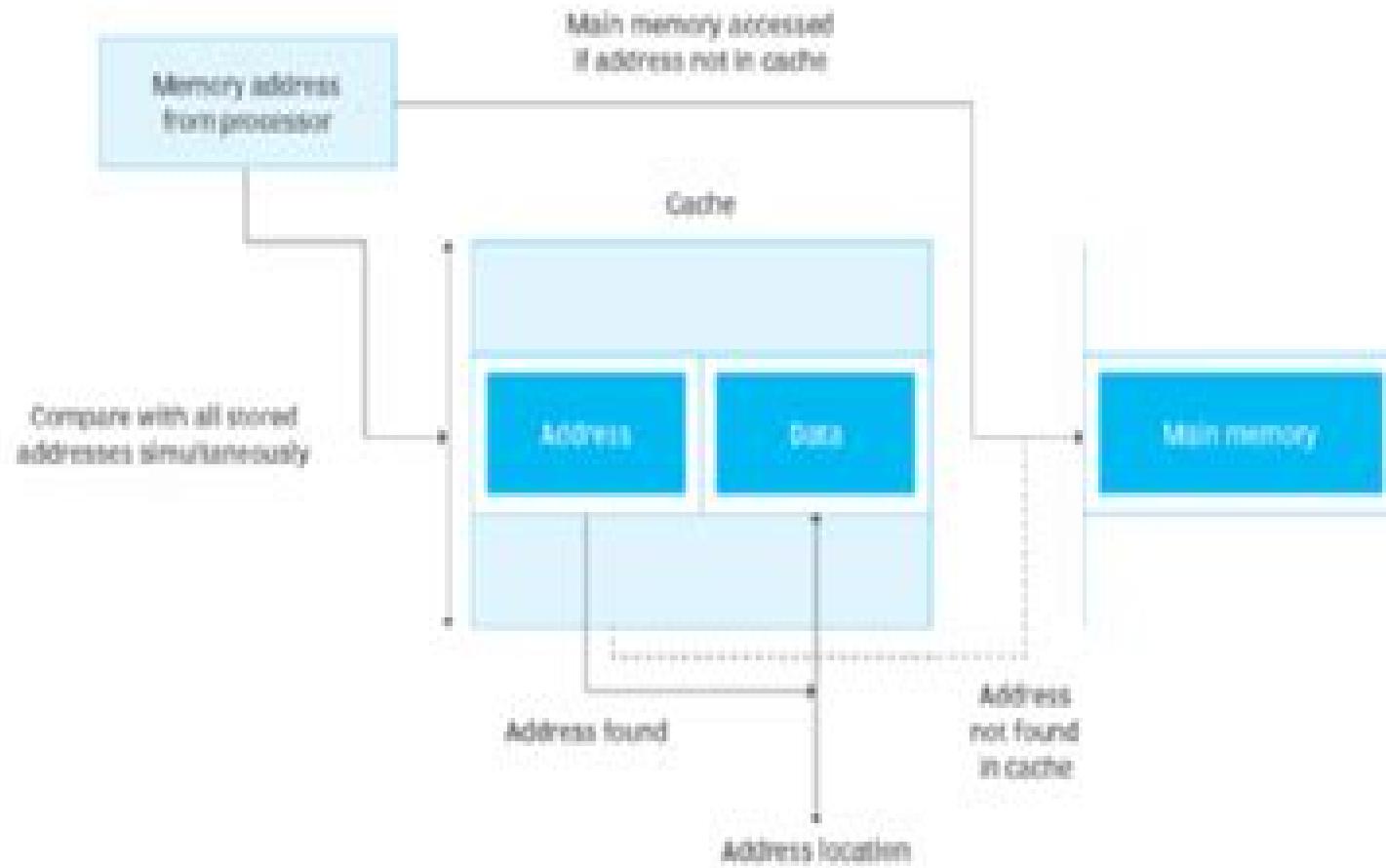


Cache memory



The Cache Memory

William Stallings

The Cache Memory:

The Cache Memory Book Jim Handy, 1998-01-13 The Second Edition of The Cache Memory Book introduces systems designers to the concepts behind cache design. The book teaches the basic cache concepts and more exotic techniques. It leads readers through some of the most intricate protocols used in complex multiprocessor caches. Written in an accessible, informal style, this text demystifies cache memory design by translating cache concepts and jargon into practical methodologies and real life examples. It also provides adequate detail to serve as a reference book for ongoing work in cache memory design. The Second Edition includes an updated and expanded glossary of cache memory terms and buzzwords. The book provides new real world applications of cache memory design and a new chapter on cachetricks. Illustrates detailed example designs of caches. Provides numerous examples in the form of block diagrams, timing waveforms, state tables, and code traces. Defines and discusses more than 240 cache specific buzzwords, comparing in detail the relative merits of different design methodologies. Includes an extensive glossary complete with clear definitions, synonyms, and references to the appropriate text discussions.

Cache and Memory Hierarchy Design Steven A. Przybylski, 1990 A widely read and authoritative book for hardware and software designers. This innovative book exposes the characteristics of performance optimal single and multi level cache hierarchies by approaching the cache design process through the novel perspective of minimizing execution time.

Cache-memory Interfaces in Compressed Memory Systems International Business Machines Corporation. Research Division. (IBMRD), Caroline D. Benveniste, Peter A. Franaszek, John T. Robinson, 2000 Abstract We consider a number of cache memory hierarchy design issues in systems with compressed random access memories (C-RAMs) in which compression and decompression occur automatically to and from main memory. Using a C-RAM as main memory segments of main memory are stored in a compressed format and dynamically decompressed to handle cache misses at the next higher level of memory. Design of main memory directory structures and storage allocation methods in such systems are described elsewhere; here we focus on issues related to cache memory interfaces. In particular, if the cache line size of the cache or caches to which main memory data is transferred is different than the size of the unit of compression in main memory, bandwidth and latency problems can occur. Another issue is that of guaranteed forward progress, that is, ensuring that modified lines can be written to the compressed main memory so that the system can continue operation even if overall compression deteriorates. We study several approaches for solving these problems using trace driven analysis to evaluate alternatives.

The Cache-coherence Problem in Shared-memory Multiprocessors Milo Tomašević, Veljko Milutinović, 1993 A tutorial on the nature of the cache coherence problem and the wide variety of proposed hardware solutions currently available. A number of the most important papers in this field are included within seven sections introductory issues, memory reference characteristics of parallel programs, directo

A Primer on Compression in the Memory Hierarchy Somayeh Sardashti, Angelos Arelakis, Per Stenström, David A. Wood, 2015-12-16 This synthesis lecture

presents the current state of the art in applying low latency lossless hardware compression algorithms to cache memory and the memory cache link There are many non trivial challenges that must be addressed to make data compression work well in this context First since compressed data must be decompressed before it can be accessed decompression latency ends up on the critical memory access path This imposes a significant constraint on the choice of compression algorithms Second while conventional memory systems store fixed size entities like data types cache blocks and memory pages these entities will suddenly vary in size in a memory system that employs compression Dealing with variable size entities in a memory system using compression has a significant impact on the way caches are organized and how to manage the resources in main memory We systematically discuss solutions in the open literature to these problems Chapter 2 provides the foundations of data compression by first introducing the fundamental concept of value locality We then introduce a taxonomy of compression algorithms and show how previously proposed algorithms fit within that logical framework Chapter 3 discusses the different ways that cache memory systems can employ compression focusing on the trade offs between latency capacity and complexity of alternative ways to compact compressed cache blocks Chapter 4 discusses issues in applying data compression to main memory and Chapter 5 covers techniques for compressing data on the cache to memory links This book should help a skilled memory system designer understand the fundamental challenges in applying compression to the memory hierarchy and introduce him her to the state of the art techniques in addressing them

The Architecture of Computer Hardware Systems Software Irv Englander,1996-02-27 Most computer architecture books are just too technical and complex Focusing on specific technology they often by pass the basics and are outdated as quickly as technology advances Now you can give your students a gentle introduction to computer architecture and systems software that will provide the appropriate amount of technical detail they need to make successful decisions in their future careers This text covers the basics in an accessible easy to understand way Organized in a form that parallels an actual computer system entire sections are devoted to principles of data hardware and software to emphasize the importance of computer structure Assuming only basic knowledge these sections build up to an in depth understanding of each topic and how they interrelate to make up a computer system

SPARC RISC User's Guide Ross Technology,1990

Proceedings Tencon ,1987

Proceedings of the Trends in Electronics Conference ,1987

Implementing Persistent Object Bases Alan

Dearle,Gail M. Shaw,Stanley Benjamin Zdonik,1991

Microcomputer Products Handbook ,1992

Electronics ,1984

Peter Norton's Peter Norton,2002-11 Peter Norton's Essential Concepts 5th Edition is a state of the art text that provides comprehensive coverage of computer concepts It is geared toward students learning about computer systems for the first time Some of the topics covered are an Overview of computers input methods and output devices processing data storage devices operating systems software networking Internet resources and graphics

Computer Organization and Architecture William Stallings,1987

Power RISC System/6000 Dipto Chakravarty,1994 This book is designed to serve

as a single reference source for the POWER RS 6000 family of workstations Starting with a comprehensive overview of hardware and software concepts from a user's perspective the book then focuses on the facilities available in the operating system and hardware subsystems from a systems point of view Hewlett-Packard Journal ,1950 *Critical Words Cache Memory* ,2008 The major constraints on increasing computer performance are power dissipation and memory latency These have led to increases in secondary cache memory L2 capacity to minimize the occurrence of power intensive and slow off chip main memory accesses However as they have grown secondary cache memories have become a large part of the total processor power dissipation and their access time has increased in terms of processor clock cycles Most cache memory architecture research has focused on primary cache memory L1 or the overall cache hierarchy In contrast architectural improvements of the L2 have usually been simple increases in capacity and associativity Our research concerns two previously unexamined attributes of L1 misses and a novel architectural means to reduce the average hit time and power dissipation of L2 designs without negatively impacting their hit rates We investigate both a form of sequence regularity in L1 miss streams and the quantity of critical words within cache blocks as indicators of the potential for memory hierarchy speed and power improvements resulting from segregating the L2 treatment of so called critical and non critical words We call the form of sequence regularity critical word regularity CWR the amount of critical words within cache blocks critical footprint size CFS and cache memories with architectures that exploit CWR and CFS we call critical words cache CW memories We describe practical CW architectures operating methods and implementation approaches We show that CW memories offer dramatically higher performance than standard cache architectures employing the well known critical word first bus protocols Our investigation consisted of four major phases each of which employed a trace driven cache simulation experiment The goal of the first phase was to determine whether significant CWR exists in the load miss stream of a primary data cache memory L1D Having found this to be the case initial estimates of potential CW performance were made The second phase sought to quantify the CWR and CFS in the load miss streams of the SPEC CPU 2000 collection of benchmark applications across nine L1D configurations The CWR results of the second experiment were then used to estimate both secondary CW coverage of L1D load misses and the overall performance of a computer system with a memory hierarchy that includes a CW The third phase of our investigation built on the second and more completely measured CWR and CFS The range of benchmarks was expanded in the third phase experiment and the CWR of instruction fetch misses and data store misses were measured in addition to that of data load misses The CFS distributions were also measured to better estimate the resource requirements for practical CW memories The fourth and final phase of our investigation determined the workload performance improvements obtainable with practical CW memories of various capacities configurations operating methods and implementations We also further explored the cost and performance tradeoffs made possible by exploitation of CWR and CFS using a CW secondary cache architecture Our investigation shows that sufficient CWR exists in both data and

instruction miss streams for the segregation of the critical words in L2 blocks to be worthwhile. The average CWR for all miss types in both SPEC CPU 2000 and 2006 workloads was found to range from almost 40% up to 90% across a wide range of L1 configurations. CWR was found to depend primarily on the workload and secondarily on the cache configuration. We also found that on average more than half of all cache blocks that are repeatedly missed in a L1 have only one critical word even in L1 designs composed of large 128 byte blocks. With one exception in all of the L1 configurations we examined only one quarter of the words were ever critical words in more than 77% of the repeatedly missed cache blocks in the data load miss streams. We used our CWR and CFS results to estimate that exploitation of criticality in L1 miss streams by using a secondary CW has the potential to cover more than 60% of L1D load misses more quickly and efficiently than standard architecture cache memories. Several practical CW configurations were found that achieve average L2 hit coverage in excess of 70%. CW hit coverage was also found to scale well generally increasing with overall cache capacity. The CW architecture offers significant reductions in both L2 average access time and dynamic power consumption. Our timing power and area estimates of practical CW memories indicate that the CW architecture is more power and area efficient for a small 128KB capacity L2. However a small capacity CW offers no system level execution time advantage over the standard serial L2 architecture. In contrast the CW advantages for a large capacity L2 are profound. For example compared to an 8MB capacity standard serial access cache memory a comparable CW would be more than 25% faster while using 76% less energy per hit access and occupying 62% less area. Another 8MB CW configuration would use 40% less energy per hit access, occupy 63% less die area and be 32% faster while dissipating only 3% worse leakage power than the comparable standard serial cache memory. If these CW memories replaced a standard architecture critical word first 8MB L2 in a high performance computer system the resulting system would respectively be 19% and 22% faster. We also show that secondary CW memories provide significant architectural flexibility enabling smaller faster and more power efficient cache memories to be used without degrading overall memory hierarchy performance or efficiency. In turn smaller and thus lower latency cache memories may enable simpler e.g. single threaded in order processor cores to be used. Taken together all these architectural possibilities would yield significantly more power efficient and higher performance computers for the same cost and fabrication technology.

80486 System Architecture Tom Shanley, MindShare, Inc, 1995. 80486 System Architecture describes the hardware architecture of PC products using the Intel family of 80486 chips providing a clear concise explanation of the 80486 processor's relationship to the rest of the system. The author provides a comprehensive treatment of the processor including 80486 microarchitecture and its functional units, internal and external caches, hardware interface, SL technology features, instructions new to the 80486, the register set, 486, 487SX processors, 486DX2 processors, 486DX2 write back enhanced processor, 486DX4 processors, implementation specific issues, main memory subsystem design, OverDrive processors. If you design or test hardware or software that involves 486 processors, 80486 System Architecture is an essential time saving tool.

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