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FIFTH EDITION

Solid State Electronic Devices

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Department of Electrical and Computer Engineering
The University of Texas at Austin*



Multi-level copper metallization: of a complementary metal oxide semiconductor (CMOS) chip. This scanning electron micrograph (scale: $1 \mu\text{m} = 3.5 \text{ microns}$) of a CMOS integrated circuit shows six levels of copper metallization that are used to carry electrical signals on the chip. The intermetal dielectric insulators have been chemically etched away here to reveal the copper. Inset: cross-section micrograph courtesy of IBM.



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Solid State Electronic Amplifiers An Empirical Approach

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