SOFTWARE SYNTHESIS FROM DATAFLOW GRAPHS

Edited by

Jonathan Allen

Software Synthesis From Dataflow Graphs

Praveen K. Murthy,Shuvra S. Bhattacharyya

Software Synthesis From Dataflow Graphs:

Software Synthesis from Dataflow Graphs Shuvra S. Bhattacharyya,Praveen K. Murthy,Edward A. Lee,2012-12-06 Software Synthesis from Dataflow Graphs addresses the problem of generating efficient software implementations from applications specified as synchronous dataflow graphs for programmable digital signal processors DSPs used in embedded real time systems The advent of high speed graphics workstations has made feasible the use of graphical block diagram programming environments by designers of signal processing systems A particular subset of dataflow called Synchronous Dataflow SDF has proven efficient for representing a wide class of unirate and multirate signal processing algorithms and has been used as the basis for numerous DSP block diagram based programming environments such as the Signal Processing Workstation from Cadence Design Systems Inc COSSAP from Synopsys both commercial tools and the Ptolemy environment from the University of California at Berkeley A key property of the SDF model is that static schedules can be determined at compile time This removes the overhead of dynamic scheduling and is thus useful for real time DSP programs where throughput requirements are often severe Another constraint that programmable DSPs for embedded systems have is the limited amount of on chip memory Off chip memory is not only expensive but is also slower and increases the power consumption of the system hence it is imperative that programs fit in the on chip memory whenever possible Software Synthesis from Dataflow Graphs reviews the state of the art in constructing static memory optimal schedules for programs expressed as SDF graphs Code size reduction is obtained by the careful organization of loops in the target code Data buffering is optimized by constructing the loop hierarchy in provably optimal ways for many classes of SDF graphs The central result is a uniprocessor scheduling framework that provably synthesizes the most compact looping structures called singleappearance schedules for a certain class of SDF graphs In addition algorithms and heuristics are presented that generate single appearance schedules optimized for data buffering usage Numerous practical examples and extensive experimental data are provided to illustrate the efficacy of these techniques **Handbook of Signal Processing Systems** Shuvra S. Bhattacharyya,Ed F. Deprettere,Rainer Leupers,Jarmo Takala,2013-06-20 Handbook of Signal Processing Systems is organized in three parts The first part motivates representative applications that drive and apply state of the art methods for design and implementation of signal processing systems the second part discusses architectures for implementing these applications the third part focuses on compilers and simulation tools describes models of computation and their associated design tools and methodologies This handbook is an essential tool for professionals in many fields and researchers of all levels **Memory Management for Synthesis of DSP Software** Praveen K. Murthy,Shuvra S. Bhattacharyya,2018-12-14 Although programming in memory restricted environments is never easy this holds especially true for digital signal processing DSP The data rich computation intensive nature of DSP makes memory management a chief and challenging concern for designers Memory Management for Synthesis of DSP Software focuses on minimizing memory requirements

during the synthesis of DSP software from dataflow representations Dataflow representations are used in many popular DSP design tools and the methods of this book can be applied in that context as well as other contexts where dataflow is used This book systematically reviews research conducted by the authors on memory minimization techniques for compiling synchronous dataflow SDF specifications Beginning with an overview of the foundations of software synthesis techniques from SDF descriptions it examines aggressive buffer sharing techniques that take advantage of specific and quantifiable tradeoffs between code size and buffer size to achieve high levels of buffer memory optimization The authors outline coarse level strategies using lifetime analysis and dynamic storage allocation DSA for efficient buffer sharing as one approach and demonstrate the role of the CBP consumed before produced parameter at a finer level using a merging framework for buffer sharing They present two powerful algorithms for combining these sharing techniques and then introduce techniques that are not restricted to the single appearance scheduling space of the other techniques Extensively illustrated to clarify the mathematical concepts Memory Management for Synthesis of DSP Software presents a comprehensive survey of state of the art research in DSP software synthesis   *EDA for IC System Design, Verification, and Testing* Louis Scheffer,Luciano Lavagno,Grant Martin,2018-10-03 Presenting a comprehensive overview of the design automation algorithms tools and methodologies used to design integrated circuits the Electronic Design Automation for Integrated Circuits Handbook is available in two volumes The first volume EDA for IC System Design Verification and Testing thoroughly examines system level design microarchitectural design logical verification and testing Chapters contributed by leading experts authoritatively discuss processor modeling and design tools using performance metrics to select microprocessor cores for IC designs design and verification languages digital simulation hardware acceleration and emulation and much more Save on the complete set

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architectures systolic algorithms and architectures rapid prototyping design methodolgies and compilers

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CASES ... ,2005   **Proceedings of the 2000 Congress on Evolutionary Computation** Institute of Electrical and Electronics Engineers,2000 These volumes contain the proceedings of the 2000 Congress on Evolutionary Computation The papers address genetic programming evolutionary optimization the evolution of neural networks evolutionary robotics data mining with evolutionary algorithms bio inspired hardware and more   Task Allocation and Scheduling of Concurrent Applications to Multiprocessor Systems Kaushik Ravindran,2007   Fourth IEEE Real-Time Technology and Applications Symposium ,1998 This volume addresses topics including scheduling communication methodologies and architectures operating systems and middleware quality of service specification and verification database and information systems and experiences and case studies

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web softball pitchers must use an underhand motion to pitch throwing the ball from under their arms baseball pitchers may use any method though overhand throws are most commonly used number of innings per game softball games are made up of seven innings while baseballers must play nine per game