Testing Static Random Access Memories

Defects, Fault Models and Test Patterns

by

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Testing Static Random Access Memories:

   Testing Static Random Access Memories Said Hamdioui,2004-03-31 Embedded memories are one of the fastest growing segments oftoday s new technology market According to the 2001 InternationalTechnology Roadmap for Semiconductors embedded memories will continueto dominate the increasing system on chip SoC content in the nextseveral years approaching 94% of the SoC area in about 10 years Furthermore the shrinking size of manufacturing structures makesmemories more sensitive to defects Consequently the memory yieldwill have a dramatic impact on the overall Defect per million level hence on the overall SoC yield Meeting a high memory yield requiresunderstanding memory designs modeling their faulty behaviors designing adequate tests and diagnosis algorithms as well as efficientself test and repair schemes Testing Static Random Access Memories covers testing of one ofthe important semiconductor memories types it address testing ofstatic random access memories SRAMs both single port andmulti port It contributes to the technical acknowledge needed bythose involved in memory testing engineers and researchers The bookbegins with outlining the most popular SRAMs architectures Then thedescription of realistic fault models based on defect injection andSPICE simulation are introduced Thereafter high quality and lowcost test patterns as well as test strategies for single port two port and any p port SRAMs are presented together with somepreliminary test results showing the importance of the new tests inreducing DPM level The impact of the port restrictions e g read only ports on the fault models tests and test strategies isalso discussed Features   **High Performance Memory Testing** R. Dean Adams,2002-09-30 Are memory applications more critical than they have been in the past Yes but even more critical is the number of designs and the sheer number of bits on each design It is assured that catastrophes which were avoided in the past because memories were small will easily occur if the design and test engineers do not do their jobs very carefully High Performance Memory Testing Design Principles Fault Modeling and Self Test is based on the author s 20 years of experience in memory design memory reliability development and memory self test High Performance Memory Testing Design Principles Fault Modeling and Self Test is written for the professional and the researcher to help them understand the memories that are being tested   **Digital Logic Testing and Simulation** Alexander Miczo,2003-10-10 Your road map for meeting today s digital testing challenges Today digital logic devices are common in products that impact public safety including applications in transportation and human implants Accurate testing has become more critical to reliability safety and the bottom line Yet as digital systems become more ubiquitous and complex the challenge of testing them has become more difficult As one development group designing a RISC stated the work required to test a chip of this size approached the amount of effort required to design it A valued reference for nearly two decades Digital Logic Testing and Simulation has been significantly revised and updated for designers and test engineers who must meet this challenge There is no single solution to the testing problem Organized in an easy to follow sequential format this Second Edition familiarizes the reader with the many different strategies for testing and their applications and

assesses the strengths and weaknesses of the various approaches The book reviews the building blocks of a successful testing strategy and guides the reader on choosing the best solution for a particular application Digital Logic Testing and Simulation Second Edition covers such key topics as Binary Decision Diagrams BDDs and cycle based simulation Tester architectures Standard Test Interface Language STIL Practical algorithms written in a Hardware Design Language HDL Fault tolerance Behavioral Automatic Test Pattern Generation ATPG The development of the Test Design Expert TDX the many obstacles encountered and lessons learned in creating this novel testing approach Up to date and comprehensive Digital Logic Testing and Simulation is an important resource for anyone charged with pinpointing faulty products and assuring quality safety and profitability   **Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits** M. Bushnell,Vishwani Agrawal,2006-04-11 The modern electronic testing has a forty year history Test professionals hold some fairly large conferences and numerous workshops have a journal and there are over one hundred books on testing Still a full course on testing is offered only at a few universities mostly by professors who have a research interest in this area Apparently most professors would not have taken a course on electronic testing when they were students Other than the computer engineering curriculum being too crowded the major reason cited for the absence of a course on electronic testing is the lack of a suitable textbook For VLSI the foundation was provided by semiconductor device techn ogy circuit design and electronic testing In a computer engineering curriculum therefore it is necessary that foundations should be taught before applications The field of VLSI has expanded to systems on a chip which include digital memory and mixed signalsubsystems To our knowledge this is the first textbook to cover all three types of electronic circuits We have written this textbook for an undergraduate foundations course on electronic testing Obviously it is too voluminous for a one semester course and a teacher will have to select from the topics We did not restrict such freedom because the selection may depend upon the individual expertise and interests Besides there is merit in having a larger book that will retain its usefulness for the owner even after the completion of the course With equal tenacity we address the needs of three other groups of readers   Mathematical and Engineering Methods in Computer Science Antonin Kucera,Thomas A. Henzinger,Jaroslav Nešetřil,Tomas Vojnar,David Antos,2013-01-17 This volume contains the post proceedings of the 8th Doctoral Workshop on Mathematical and Engineering Methods in Computer Science MEMICS 2012 held in Znojmo Czech Republic in October 2012 The 13 thoroughly revised papers were carefully selected out of 31 submissions and are presented together with 6 invited papers The topics covered by the papers include computer aided analysis and verification applications of game theory in computer science networks and security modern trends of graph theory in computer science electronic systems design and testing and quantum information processing   **VLSI Test Principles and Architectures** Laung-Terng Wang,Cheng-Wen Wu,Xiaoqing Wen,2006-08-14 This book is a comprehensive guide to new DFT methods that will show the readers how to design a testable and quality product drive down test cost improve product quality and yield and speed up time to market and

time to volume Most up to date coverage of design for testability Coverage of industry practices commonly found in commercial DFT tools but not discussed in other books Numerous practical examples in each chapter illustrating basic VLSI test principles and DFT architectures *CMOS SRAM Circuit Design and Parametric Test in Nano-Scaled Technologies* Andrei Pavlov,Manoj Sachdev,2008-06-01 The monograph will be dedicated to SRAM memory design and test issues in nano scaled technologies by adapting the cell design and chip design considerations to the growing process variations with associated test issues Purpose provide process aware solutions for SRAM design and test challenges **Records of the 2003 IEEE International Workshop on Memory Technology, Design and Testing, 28-29 July, 2003, San Jose, California** Tom Wit,Adit Singh,Rochit Rajsuman,2003 IEEE Computer Society Order Number PR02004 T p verso **Records of the 1993 IEEE International Workshop on Memory Testing, August 9-10, 1993, San Jose, California** Rochit Rajsuman,1993 From the August 1993 workshop in San Jose California 26 papers report the latest findings on testing computer memory The sections include test pattern generation algorithms fault models testing for process defects and yield improvement and radiation issues and space applications No subject i Records of the 2002 IEEE International Workshop on Memory Technology, Design and Testing Bernard Courtois,Thomas Wik,Yervant Zorian,2002 Annotation MTDT 2002 explores the state of the art in semiconductor memories Over the last 10 years the scope of the Workshop has been expanded to cover the fabrication technology and the memory design test and reliability *International Test Conference, 1992* Institute of Electrical and Electronics Engineers,1992 Annotation The proceedings of the 23rd edition of the premier technical conference on electronic testing held in Baltimore Maryland September 1992 comprise papers panels and tutorials in the areas of design and test integration test management software test hardware device assembly and system test and IEEE test standards ITC s 1992 theme Discover the New World of Test and Design reflects the growing emphasis on tighter integration of test and design to assure the highest quality products No subject index Ruggedly bound for heavy use Annotation copyrighted by Book News Inc Portland OR **IEEE VLSI Test Symposium** ,2005 **Review of Industrial Organization** ,1998 **N.S.C. Review** ,1976 **Australian Official Journal of Trade Marks** ,2003-01-02 **American Book Publishing Record** ,2004 **Proceedings** ,1995 STI Review ,1989 *Unfair Competition and the ITC* ,1993 Japan Telecommunications Review ,1986

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