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## Combined Graduate Level Examination (Tier-II), 2018

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| Name             |                                                             |
| Test Venue       | SSC Digital Zone (D) Jaipur                                 |
| Test Date        | 21.07.2018 - 12:00 PM                                       |
| Test Code        | 2018-2019                                                   |
| Subject          | SSC Tier II Paper for General Studies Finance and Economics |

Section - Part A: Finance and Economics

Q1. A trial balance may be prepared according to \_\_\_\_\_ Method and \_\_\_\_\_ Method.

- Ans. ☒ 1. Double  
☒ 2. Partial  
☒ 3. Single  
☒ 4. None

Question ID: 200007193  
Status: Marked For Review  
Correct Option: 1

Q2. \_\_\_\_\_ appears on the credit side of Manufacturing Account.

- Ans. ☒ 1. Purchase of raw material

\_\_\_\_\_ price of materials or goods which have been consumed but not yet received.

- Ans. ☒ 1. Purchase of raw material  
☒ 2. Issue of raw material  
☒ 3. Purchase of finished goods  
☒ 4. Issue of finished goods

Question ID: 200007194  
Status: Marked For Review  
Correct Option: 1

Q3. A manufacturer can find out what his business costs and what it owes from \_\_\_\_\_.

- Ans. ☒ 1. Trade Account  
☒ 2. Balance Sheet  
☒ 3. Ledger  
☒ 4. Trading A/c

Question ID: 200007195  
Status: Answered  
Correct Option: 2

Q4. The maker of a bill of exchange is called the \_\_\_\_\_.

- Ans. ☒ 1. Drawee

# Question Out Ssc

**Clemens Wendtner**



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web jul 7 2017 i have the following code for a 2 bit multiplier module multiplier a0 a1 b0 b1 c 3 0 output 3 0 c input a0 a1 b0 b1 wire a0b1 a1b0 ha0c a1b1 and c 0 a0

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web mar 28 2020 a multiplier is a circuit that takes two numbers as input and produces their product as an output so a binary multiplier takes binary numbers as inputs and produces a result in binary before moving forward lets quickly recap binary multiplication first 0 x 0 0 0 x 1 0 1 x 0 0 1 x 1 1 so there s always a confusion in students

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web the verilog arithmetic operators all produce full precision results e g adding two 8 bit numbers produces a 9 bit result in many designs one chooses a word size many computers use 32 or 64 bits and all arithmetic results are truncated to that number of bits i e arithmetic is performed modulo 2word size

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web sequential multiplier assume the multiplicand a has n bits and the multiplier b has m bits if we only want to invest in a single n bit adder we can build a sequential circuit that processes a single partial product at a time and then cycle the circuit m times p b a s n nc n xn n n 1 s n 1 s 0 init p 0 load a and b repeat m times

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web apr 9 2015 for your 4 input multiplier you will probably want to use bit concatenation to form the input bits wire 3 0 a wire 3 0 b case a b endcase and your case statement will have 256 lines in it

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web apr 15 2021 1 i am trying to implement a 4 bit signed sequential multiplier i have a for loop in my tb but only the multiplicand changes not the multiplier when i manually change the multiplier i notice that my product outputs all 0s then it changes to the actual product what am i doing wrong

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web aug 30 2020 i m designing an 8 bit signed sequential multiplier using verilog the inputs are clk clock rst reset a 8 bit multiplier b 8 bit multiplicand and the outputs are p product and rdy ready signal indicating multiplication is over

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web you cannot use the multiplication operator of verilog the lab file submission deadline is on 9 28 by 6 00pm write simulation for a multiplier the input output ports of the 8 bit multiplier is as follows module seqmultiplier input wire clk input wire enable input wire 7 0 a input wire 7 0 b output wire 15 0 c