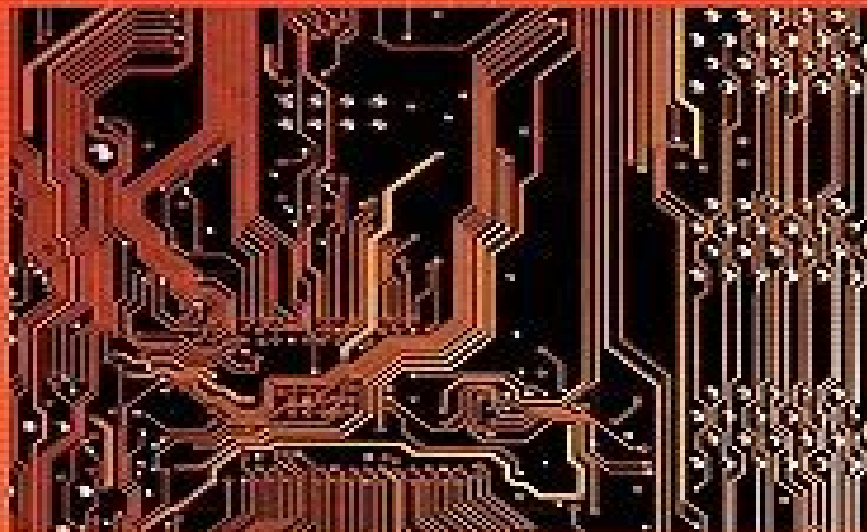


Symbolic Analysis and Reduction of VLSI Circuits

Chung-Kuan Cheng, Zhanhai Qin and Sheldon Tan



Symbolic Analysis And Reduction Of Vlsi Circuits

Mourad Fakhfakh, Esteban Tlelo-Cuautle, Francisco V. Fernández

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Symbolic Analysis and Reduction of VLSI Circuits Zhanhai Qin, Chung-Kuan Cheng, 2009-03-13 Symbolic analysis is an intriguing topic in VLSI designs. The analysis methods are crucial for the applications to the parasitic reduction and analog circuit evaluation. However, analyzing circuits symbolically remains a challenging research issue. Therefore, in this book, we survey the recent results as the progress of on-going works rather than as the solution of the field. For parasitic reduction, we approximate a huge amount of electrical parameters into a simplified RLC network. This reduction allows us to handle very large integrated circuits with given memory capacity and CPU time. A symbolic analysis approach reduces the circuit according to the network topology. Thus, the designer can maintain the meaning of the original network and perform the analysis hierarchically. For analog circuit designs, symbolic analysis provides the relation between the tunable parameters and the characteristics of the circuit. The analysis allows us to optimize the circuit behavior. The book is divided into three parts. Part I touches on the basics of circuit analysis in time domain and in s domain. For an s domain expression, the Taylor s expansion with s approaching infinity is equivalent to the time domain solution after the inverse Laplace transform. On the other hand, the Taylor s expansion when s approaches zero derives the moments of the output responses in time domain. Part II focuses on the techniques for parasitic reduction. In Chapter 2, we present the approximation methods to match the first few moments with reduced circuit orders. In Chapter 3, we apply the Y-Delta transformation to reduce the dynamic linear network. The method finds the exact values of the low-order coefficients of the numerator and denominator of the transfer function and thus matches part of the moments. In Chapter 4, we handle two major issues of the Y-Delta transformation: common factors in fractional expressions and round-off errors. Chapter 5 explains the stability of the reduced expression; in particular, the Ruth-Hurwitz Criterion. We make an effort to describe the proof of the Criterion because the details are omitted in most of the contemporary textbooks. In Chapter 6, we present techniques to synthesize circuits to approximate the reduced expressions after the transformation. In Part III, we discuss symbolic generation of the determinants and cofactors for the application to analog designs. In Chapter 7, we depict the classical topological analysis approach. In Chapter 8, we describe a determinant decision diagram approach that exploits the sparsity of the matrix to accelerate the computation. In Chapter 9, we take only significant terms when we search through the determinant decision diagram to approximate the solution. In Chapter 10, we extend the determinant decision diagram to a hierarchical model. The construction of the modules through the hierarchy is similar to the Y-Delta transformation in the sense that a byproduct of common factors appears in the numerator and denominator. Therefore, we describe the method to prune the common factors.

Symbolic Analysis and Reduction of VLSI Circuits Qin Zhanhai, Chung-Kuan Cheng, 2008-11-01 Symbolic analysis is an intriguing topic in VLSI designs. The analysis methods are crucial for the applications to the parasitic reduction and analog circuit evaluation. However, analyzing circuits symbolically remains a challenging research issue. Therefore, in this book, we survey the recent results as the progress

of on going works rather than as the solution of the field For parasitic reduction we approximate a huge amount of electrical parameters into a simplified RLC network This reduction allows us to handle very large integrated circuits with given memory capacity and CPU time A symbolic analysis approach reduces the circuit according to the network topology Thus the designer can maintain the meaning of the original network and perform the analysis hierarchically For analog circuit designs symbolic analysis provides the relation between the tunable parameters and the characteristics of the circuit The analysis allows us to optimize the circuit behavior The book is divided into three parts Part I touches on the basics of circuit analysis in time domain and in s domain For an s domain expression the Taylor s expansion with s approaching infinity is equivalent to the time domain solution after the inverse Laplace transform On the other hand the Taylor s expansion when s approaches zero derives the moments of the output responses in time domain Part II focuses on the techniques for parasitic reduction In Chapter 2 we present the approximation methods to match the first few moments with reduced circuit orders In Chapter 3 we apply the Y Delta transformation to reduce the dynamic linear network The method finds the exact values of the low order coefficients of the numerator and denominator of the transfer function and thus matches part of the moments In Chapter 4 we handle two major issues of the Y Delta transformation common factors in fractional expressions and round off errors Chapter 5 explains the stability of the reduced expression in particular the Ruth Hurwitz Criterion We make an effort to describe the proof of the Criterion because the details are omitted in most of the contemporary textbooks In Chapter 6 we present techniques to synthesize circuits to approximate the reduced expressions after the transformation In Part III we discuss symbolic generation of the determinants and cofactors for the application to analog designs In Chapter 7 we depict the classical topological analysis approach In Chapter 8 we describe a determinant decision diagram approach that exploits the sparsity of the matrix to accelerate the computation In Chapter 9 we take only significant terms when we search through determinant decision diagram to approximate the solution In Chapter 10 we extend the determinant decision diagram to a hierarchical model The construction of the modules through the hierarchy is similar to the Y Delta transformation in the sense that a byproduct of common factors appears in the numerator and denominator Therefore we describe the method to prune the common factors

Advanced Symbolic Analysis for VLSI Systems Guoyong Shi, Sheldon X.-D. Tan, Esteban Tlelo Cuautle, 2014-06-19 This book provides comprehensive coverage of the recent advances in symbolic analysis techniques for design automation of nanometer VLSI systems The presentation is organized in parts of fundamentals basic implementation methods and applications for VLSI design Topics emphasized include statistical timing and crosstalk analysis statistical and parallel analysis performance bound analysis and behavioral modeling for analog integrated circuits Among the recent advances the Binary Decision Diagram BDD based approaches are studied in depth The BDD based hierarchical symbolic analysis approaches have essentially broken the analog circuit size barrier

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