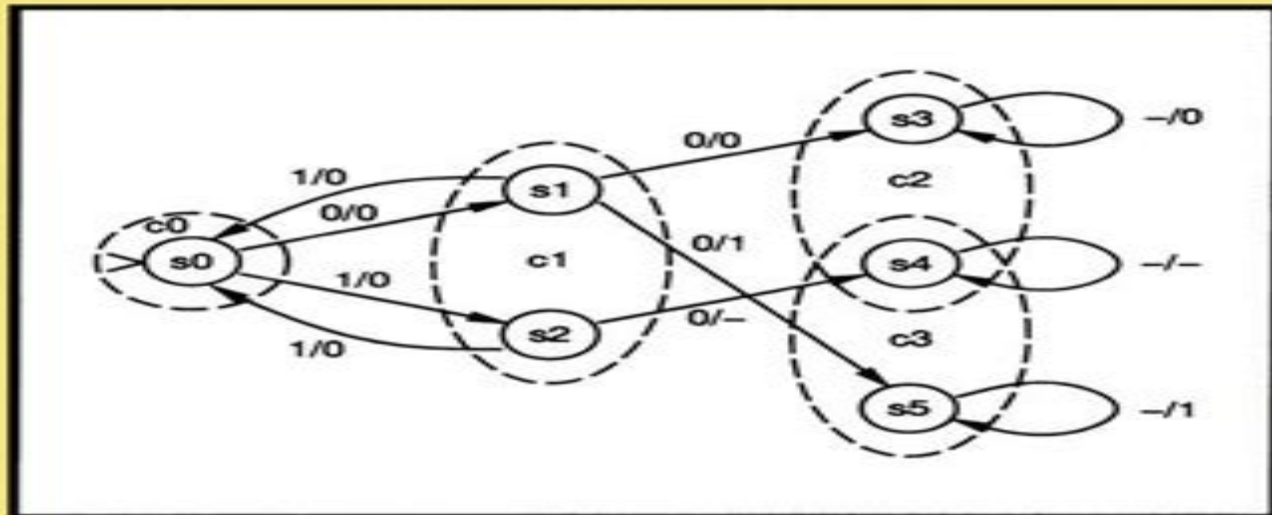


SYNTHESIS OF FINITE STATE MACHINES: Functional Optimization

Timothy Kam
Tiziano Villa
Robert Brayton
Alberto Sangiovanni-Vincentelli



Synthesis Of Finite State Machines Functional Optimization

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Synthesis Of Finite State Machines Functional Optimization:

Synthesis of Finite State Machines Timothy Kam, Tiziano Villa, Robert K. Brayton, Alberto L.

Sangiovanni-Vincentelli, 2013-03-09 Synthesis of Finite State Machines Functional Optimization is one of two monographs devoted to the synthesis of Finite State Machines FSMs This volume addresses functional optimization whereas the second addresses logic optimization By functional optimization here we mean the body of techniques that compute all permissible sequential functions for a given topology of interconnected FSMs and select a best sequential function out of the permissible ones The result is a symbolic description of the FSM representing the chosen sequential function By logic optimization here we mean the steps that convert a symbolic description of an FSM into a hardware implementation with the goal to optimize objectives like area testability performance and so on Synthesis of Finite State Machines Functional Optimization is divided into three parts The first part presents some preliminary definitions theories and techniques related to the exploration of behaviors of FSMs The second part presents an implicit algorithm for exact state minimization of incompletely specified finite state machines ISFSMs and an exhaustive presentation of explicit and implicit algorithms for the binate covering problem The third part addresses the computation of permissible behaviors at a node of a network of FSMs and the related minimization problems of non deterministic finite state machines NDFSMs Key themes running through the book are the exploration of behaviors contained in a non deterministic FSM NDFSM and the representation of combinatorial problems arising in FSM synthesis by means of Binary Decision Diagrams BDDs Synthesis of Finite State Machines Functional

Optimization will be of interest to researchers and designers in logic synthesis CAD and design automation **Synthesis of Finite State Machines** Timothy Kam, Tiziano Villa, Robert K. Brayton, 2014-01-15 *Synthesis of Finite State Machines* Tiziano Villa, Timothy Kam, Robert K. Brayton, Alberto L. Sangiovanni-Vincentelli, 2012-12-06 Synthesis of Finite State Machines Logic Optimization is the second in a set of two monographs devoted to the synthesis of Finite State Machines FSMs The first volume Synthesis of Finite State Machines Functional Optimization addresses functional optimization whereas this one addresses logic optimization The result of functional optimization is a symbolic description of an FSM which represents a sequential function chosen from a collection of permissible candidates Logic optimization is the body of techniques for converting a symbolic description of an FSM into a hardware implementation The mapping of a given symbolic representation into a two valued logic implementation is called state encoding or state assignment and it impacts heavily area speed testability and power consumption of the realized circuit The first part of the book introduces the relevant background presents results previously scattered in the literature on the computational complexity of encoding problems and surveys in depth old and new approaches to encoding in logic synthesis The second part of the book presents two main results about symbolic minimization a new procedure to find minimal two level symbolic covers under face dominance and disjunctive constraints and a unified frame to check encodability of encoding constraints and find codes of minimum length

that satisfy them The third part of the book introduces generalized prime implicants GPIs which are the counterpart in symbolic minimization of two level logic to prime implicants in two valued two level minimization GPIs enable the design of an exact procedure for two level symbolic minimization based on a covering step which is complicated by the need to guarantee encodability of the final cover A new efficient algorithm to verify encodability of a selected cover is presented If a cover is not encodable it is shown how to augment it minimally until an encodable superset of GPIs is determined To handle encodability the authors have extended the frame to satisfy encoding constraints presented in the second part The covering problems generated in the minimization of GPIs tend to be very large Recently large covering problems have been attacked successfully by representing the covering table with binary decision diagrams BDD In the fourth part of the book the authors introduce such techniques and extend them to the case of the implicit minimization of GPIs where the encodability and augmentation steps are also performed implicitly Synthesis of Finite State Machines Logic Optimization will be of interest to researchers and professional engineers who work in the area of computer aided design of integrated circuits

Synthesis of Finite State Machines Tiziano Villa, Timothy Kam, Robert K Brayton, 1997-04-01

RTL Hardware Design Using VHDL Pong P. Chu, 2006-04-20 The skills and guidance needed to master RTL hardware design This book teaches readers how to systematically design efficient portable and scalable Register Transfer Level RTL digital circuits using the VHDL hardware description language and synthesis software Focusing on the module level design which is composed of functional units routing circuit and storage the book illustrates the relationship between the VHDL constructs and the underlying hardware components and shows how to develop codes that faithfully reflect the module level design and can be synthesized into efficient gate level implementation Several unique features distinguish the book Coding style that shows a clear relationship between VHDL constructs and hardware components Conceptual diagrams that illustrate the realization of VHDL codes Emphasis on the code reuse Practical examples that demonstrate and reinforce design concepts procedures and techniques Two chapters on realizing sequential algorithms in hardware Two chapters on scalable and parameterized designs and coding One chapter covering the synchronization and interface between multiple clock domains Although the focus of the book is RTL synthesis it also examines the synthesis task from the perspective of the overall development process Readers learn good design practices and guidelines to ensure that an RTL design can accommodate future simulation verification and testing needs and can be easily incorporated into a larger system or reused Discussion is independent of technology and can be applied to both ASIC and FPGA devices With a balanced presentation of fundamentals and practical examples this is an excellent textbook for upper level undergraduate or graduate courses in advanced digital logic Engineers who need to make effective use of today's synthesis software and FPGA devices should also refer to this book

Design and Implementation of Compiler Ravendra Singh, Vivek Sharma, Manish Varshney, 2009 About the Book This well organized text provides the design techniques of compiler in a simple and straightforward manner It describes the complete development of various phases of

compiler with their imitation of C language in order to have an understanding of their application. Primarily designed as a text for undergraduate students of Computer Science and Information Technology and postgraduate students of MCA. Key Features: Chapter 1 covers all formal languages with their properties. More illustration on parsing to offer enhanced perspective of parser and also more examples in e

Modeling Time in Computing Carlo A. Furia, Dino Mandrioli, Angelo Morzenti, Matteo Rossi, 2012-10-19 Models that include a notion of time are ubiquitous in disciplines such as the natural sciences, engineering, philosophy, and linguistics, but in computing the abstractions provided by the traditional models are problematic and the discipline has spawned many novel models. This book is a systematic, thorough presentation of the results of several decades of research on developing, analyzing, and applying time models to computing and engineering. After an opening motivation introducing the topics, structure, and goals, the authors introduce the notions of formalism and model in general terms, along with some of their fundamental classification criteria. In doing so, they present the fundamentals of propositional and predicate logic and essential issues that arise when modeling time across all types of system. Part I is a summary of the models that are traditional in engineering and the natural sciences, including fundamental computer science, dynamical systems, and control theory, hardware design, and software algorithmic and complexity analysis. Part II covers advanced and specialized formalisms dealing with time modeling in heterogeneous software-intensive systems, formalisms that share finite state machines as common ancestors: Petri nets in many variants, notations based on mathematical logic such as temporal logic, process algebras, and dual language approaches combining two notations with different characteristics to model and verify complex systems, e.g., model checking frameworks. Finally, the book concludes with summarizing remarks and hints towards future developments and open challenges. The presentation uses a rigorous yet not overly technical style appropriate for readers with heterogeneous backgrounds, and each chapter is supplemented with detailed bibliographic remarks and carefully chosen exercises of varying difficulty and scope. The book is aimed at graduate students and researchers in computer science, while researchers and practitioners in other scientific and engineering disciplines interested in time modeling with a computational flavor will also find the book of value. The comparative and conceptual approach makes this a valuable introduction for non-experts. The authors assume a basic knowledge of calculus, probability theory, algorithms, and programming, while a more advanced knowledge of automata, formal languages, and mathematical logic is useful.

Intelligent Information Processing and Web Mining Mieczyslaw A. Kłopotek, Sławomir T. Wierzchon, Krzysztof Trojanowski, 2013-06-05 This volume contains articles accepted for presentation during The Intelligent Information Processing and Web Mining Conference IIS IIPWM 04, which was held in Zakopane, Poland, on May 17-20, 2004. This conference is a continuation of a series of 13 successful symposia and conferences on Intelligent Information Systems organized by the Institute of Computer Science of the Polish Academy of Sciences, devoted to new trends in broadly understood Artificial Intelligence. The idea of organizing such meetings dates back to 1992. Our main intention guided the first rather

small audience workshop in the series was to resume the results gained in Polish scientific centers as well as contrast them with the research performed by Polish scientists working at the universities in Europe and USA and their foreign collaborators This idea proved to be attractive enough that we decided to continue such meetings As the years went by the workshops has transformed into regular symposia devoted to such fields like Machine Learning Knowledge Discovery Natural Language Processing Knowledge Based Systems and Reasoning and Soft Computing i e Fuzzy and Rough Sets Bayesian Networks Neural Networks and Evolutionary Algorithms At present about 50 papers prepared by researches from Poland and other countries are usually presented This year conference devotes much more attention to the newest developments in the area of Artificial Intelligence related to broadly understood Web mining

State Minimization of Finite State Machines Using Implicit Techniques Timothy Yee-kwong Kam,1995 Proceedings ,1985 **Foundations of Embedded Systems** Alexander Barkalov,Larysa Titarenko,Małgorzata Mazurkiewicz,2019-02-04 This book is devoted to embedded systems ESs which can now be found in practically all fields of human activity Embedded systems are essentially a special class of computing systems designed for monitoring and controlling objects of the physical world The book begins by discussing the distinctive features of ESs above all their cybernetic physical character and how they can be designed to deliver the required performance with a minimum amount of hardware In turn it presents a range of design methodologies Considerable attention is paid to the hardware implementation of computational algorithms It is shown that different parts of complex ESs could be implemented using models of finite state machines FSMs Also field programmable gate arrays FPGAs are very often used to implement different hardware accelerators in ESs The book pays considerable attention to design methods for FPGA based FSMs before the closing section turns to programmable logic controllers widely used in industry This book will be interesting and useful for students and postgraduates in the area of Computer Science as well as for designers of embedded systems In addition it offers a good point of departure for creating embedded systems for various spheres of human activity *Digest of Technical Papers* ,2001

VLSI and Computer Architecture Ravi Shankar,Eduardo B. Fernandez,2014-12-01 VLSI Electronics Microstructure Science Volume 20 VLSI and Computer Architecture reviews the approaches in design principles and techniques and the architecture for computer systems implemented in VLSI This volume is divided into two parts The first section is concerned with system design Chapters under this section focus on the discussion of such topics as the evolution of VLSI system performance and processor design considerations and VLSI system design and processing tools Part II of the book focuses on the architectural possibilities that have become cost effective with the development of VLSI circuits Topics on architectural requirements and various architectures such as the Reduced Instruction Set Extended Von Neumann Language Oriented and Microprogrammable architectures are elaborated in detail Also included are chapters that discuss the evaluation of architecture multiprocessing configurations and the future of VLSI Computer designers those evaluating computer systems researchers and students of

computer architecture will find the book very useful **Field-programmable Logic and Applications** ,1997 **EDN** ,1992 **Proceedings of the First NASA/DoD Workshop on Evolvable Hardware** Adrian Stoica,Didier Keymeulen,Jason Lohn,1999 Looks at applying evolution inspired formalisms to hardware design in order to produce self reconfigurable electronic hardware by evolutionary and genetic reconfiguration mechanisms The 35 papers cover the evolution of FPGAs digital functions analog and mixed signal circuits cellular automata and brain inspired architectures reconfiguration architectures and dynamic reconfiguration advanced reconfigurable devices applications to the design and adaptation of space sub systems and genetic algorithms applications Titles but not texts are included for the nine invited talks Authors but not subjects are indexed Annotation copyrighted by Book News Inc Portland OR *Control Abstracts* ,1967 **19th IEEE VLSI Test Symposium** ,2001 Collects 58 papers from the April May 2001 symposium that explore new approaches in the testing of electronic circuits and systems Key areas in testing are discussed such as BIST analog measurement fault tolerance diagnosis methods scan chain design memory test and diagnosis and test data compression and compaction Also on the program are sessions on emerging areas that are gaining prominence including low power testing testing high speed circuits on low cost testers processor based self test techniques and core based system on chip testing Some of the topics are robust and low cost BIST architectures for sequential fault testing in datapath multipliers a method for measuring the cycle to cycle period jitter of high frequency clock signals fault equivalence identification using redundancy information and static and dynamic extraction and test scheduling for minimal energy consumption under power constraints No subject index c Book News Inc **Twelfth International Conference on VLSI Design** VLSI Society of India,IEEE Circuits and Systems Society,1999 The proceedings of the January 1999 conference consist of 103 papers 11 talks and six tutorials The papers are grouped under the headings of TCAD to ECAD low power testing co design and synthesis analog design multi valued logic verification digital signal processor DSP logic synthesis **Computer & Control Abstracts** ,1996

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